

REMARKS**Summary of the Office Action**

Claims 1-4, 7-17, and 20-24 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Zavracky et al. (US 6,552,704) in view of Sugawara et al. (US 6,504,523).

Claims 5, 6, 18 and 19 stand objected to as being dependent on rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Summary of the Response to the Office Action

Claims 4, 5, 12, 13, 15, 17, and 24 have been amended to correct minor typographical errors. No new matter has been added. Claims 1-24 are currently pending for further consideration.

Allowable Subject Matter

Applicants wish to thank the Examiner for indicating that claims 5, 6, 18 and 19 contain allowable subject matter. However, because the Applicants respectfully submit that claims 1-4, 7-17, and 20-24 are also allowable for the reasons stated below, these claims have not been written in independent form at this time.

Premature Finality of Office Action

Applicants respectfully assert that the finality of the present Office Action is premature and thus requests that the finality of the present Office Action be withdrawn. Applicants respectfully assert that although the same references cited in the previous Office Action may have been used in the present Office Action, the rejections are based on *new grounds of rejection*.

In particular, in the first Office Action after RCE (issued March 22, 2005), the §103 rejection was based, in part, on Sugawara et al. allegedly teaching the claimed “reference common voltage” as $V_{com}=5V$, “high-level common voltage” as $V_{gon}=19V$, and “low level common voltage” as $V_{goff}=-10V$. *See* OA (3/22/05) at bottom of page 2 and top of page 3 citing to FIGs. 3 and 10. In the present Office Action, the same recited elements are now allegedly taught in Sugawara et al. based on *completely different voltages*; mainly, “reference common voltage” as $V_{com}=0V$, “high-level common voltage” as $V_{com}=5V$, and “low level common voltage” as $V_{com}=-5V$. *See* FOA (11/1/05) at top of page 3 citing to FIG. 9.

MPEP 21706.07(a) states:

Under present practice, second or any subsequent actions on the merits shall be final, **except** where the examiner introduces *a new ground of rejection* that is neither necessitated by applicant’s amendment of the claims nor based on information submitted in an information disclosure statement.... (emphasis added).

Applicants did not amend any claims or introduce any information disclosure statement in the previous response. Moreover, the rejection of claims 1-4, 7-17, and 20-24 presented in the present Office Action does not further explain the bases of the previously made rejection.

Rather, the present rejections are based on *entirely different grounds presented for the first time*. As Applicants are entitled to a full and fair hearing (MPEP §706.07), Applicants respectfully submit that the rejections presented now are based on new grounds of rejection and are therefore *prematurely made final*. Hence, Applicants respectfully request that the finality of the Office Action be withdrawn and the claims reconsidered based on the following remarks.

All Claims Comply with §103

Claims 1-4, 7-17, and 20-24 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Zavracky et al. (US 6,552,704) in view of Sugawara et al. (US 6,504,523). Applicants respectfully disagree for the following reasons.

As discussed in depth in the previous response and incorporated herein by reference, Zavracky et al. does not teach or even suggest at least the step of “applying a reference common voltage to the plurality of liquid crystal cells after applying the one of the high-level common voltage and the low-level common voltage” as recited in independent claim 1 or the step of “applying a reference common voltage to the plurality of the liquid crystal cells after the allowing of the liquid crystal cells to respond” as recited in independent claim 13. (See previous Request for Reconsideration: page 3, first full paragraph.) The Office Action now asserts that Sugawara et al. teaches such steps based on FIG. 9 (i.e., rather than FIGs. 3 and 10 as asserted in the previous Office Action).

In particular, the Office Action now asserts that Sugawara et al. teaches “applying a reference common voltage ($V_{com}=0V$ from the time of t_{14} to t_{15}) to the plurality of liquid crystal cells after applying the one of the high-level common voltage ($V_{com}=5V$ before the time t_{13}) and low level common voltage ($V_{com}=-5V$ from the time of t_{13} to t_{14}).” (See FOA: page 3, top of page.) Applicants respectfully assert that these voltages do correspond to the recited limitations in independent claims 1 and 13 and have been taken out of context.

As an initial matter, Sugawara et al. is directed to preventing flicker when an LCD display device switches from one display mode (e.g., SXGA) to another (e.g., VGA). (See col. 1, lns. 25-29; col. 4, lns. 11-12.) This is more explicitly shown in FIG. 5, which depicts the

video signal processor 20 having a switch 22 between “Input A” and “Input B” to select the input source to the video signal processor 20. Based on this background, FIG. 9 of Sugawara et al. illustrates the signal diagram of various signals being generated by the control signal generator 62 and the switching section 64 (FIG. 8). Specifically, Sugawara et al. describes the common voltage (Vcom) generated by the switching section 64 having either a high level (5V) or a low level (-5V). The “0V” results in a state in which there is no power being supplied to the LCD when the display mode is being switched (i.e., the switch 66 is floatings). (See col. 6, lns. 59-60.) Applicants respectfully assert that this “0V” is not a “reference common voltage” as recited in independent claims 1 and 13.

Both independent claims 1 and 13 recite, in part, “a method of driving a liquid crystal display device *during one frame*.” (Emphasis added.) Furthermore, independent claim 1 recites, in part, steps of “applying one of a high-level common voltage and a low-level common voltage to a plurality of liquid crystal cells of the liquid crystal display device to write data into the liquid crystal cells within a time interval shorter than *one display frame interval*, applying a *reference common voltage* to the plurality of liquid crystal cells *after applying the one of the high-level common voltage and the low-level common voltage*, and turning on a backlight after said data writing to display an image” (emphasis added). Sugawara et al. does not teach any such features.

In Sugawara et al., the judgement section 60 determines if there is an input signal being applied to the data lines and generates a judgement signal POWC (i.e., 5V for inactive level, 0V for absence of input)(col. 6, lns. 47, 55-57). Based on the POWC signal, the switch section 64 generates a Vcom between 5V and -5V “for normal operations and assumes zero volt if the power source is off” (col. 6, lns. 57-60). In other words, the “0V” is generated when power is

not being supplied to the LCD to suspend the displaying of an image. Accordingly, Sugawara et al. does not teach or even suggest “a method of driving a liquid crystal display device *during one frame* comprising...applying a reference common voltage to the plurality of liquid crystal cells after applying the one of the high-level common voltage and the low-level common voltage” (emphasis added) as recited in independent claim 1.

Similarly, claim 13 recites, in part, “a method of driving a liquid crystal display device *during one frame* comprising...inputting data signals to a plurality of liquid crystal cells, allowing the liquid crystal cells to respond to the applied data signals, and applying a reference common voltage to the plurality of the liquid crystal cells after the allowing of the liquid crystal cells to respond” (emphasis added). As explained above, the “0V” generated by the switch section 64 in Sugawara et al. is not “a reference common voltage” as recited in claim 13 as Sugawara et al. does not teach or even suggest the recited steps.

In conclusion, Applicants respectfully assert that Sugawara et al. does not teach or suggest at least the features discussed above. Moreover, Applicants further assert that the signal diagram of FIG. 9 is not even related to the “method of driving a liquid crystal display device during one frame” as recited in independent claims 1 and 13. Rather, Sugawara et al. is directed to preventing flicker when an LCD device is switched from one display mode to another.

In addition, Applicants respectfully assert that even if Zavracky et al. is combined with Sugawara et al., the combination still fails to teach the recited features of claims 1 and 13. At best, the combination of Zavracky et al. and Sugawara et al. would teach applying the judging/switching steps related to reducing flicker when the LCD device of Zavracky et al. switches from one display mode to another as taught by Sugawara et al., the $V_{com}=0V$ being

generated when there is no power to the LCD. Applicants respectfully assert that such a combination would still fail to teach at least “a method of driving a liquid crystal display device *during one frame* comprising...applying a *reference common voltage* to the plurality of liquid crystal cells *after applying the one of the high-level common voltage and the low-level common voltage*, and turning on a backlight after said data writing to display an image” (claim 1) or “a method of driving a liquid crystal display device *during one frame* comprising...inputting data signals to a plurality of liquid crystal cells, allowing the liquid crystal cells to respond to the applied data signals, and applying *a reference common voltage* to the plurality of the liquid crystal cells *after the allowing of the liquid crystal cells to respond*” (claim 13).

Accordingly, Applicants respectfully assert that Zavracky et al. and Sugawara et al., whether taken individually or in combination, fail to teach or suggest the features of independent claims 1 and 13 for at least the reasons stated above. As dependent claims 2-4, 7-12, 14-17, and 20-24 all depend either from independent claim 1 or 13, Applicants respectfully assert that Zavracky et al. and Sugawara et al., whether taken individually or in combination, also fail to teach the recited features for at least the reasons explained above. Hence, Applicants respectfully request that the §103 rejection be withdrawn.

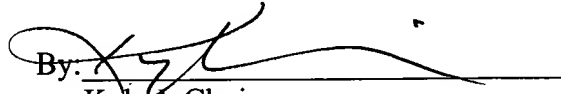
CONCLUSION

In view of the foregoing, Applicants respectfully request reconsideration and timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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